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CHIP-SCALE SIMULATION OF RESIDUAL LAYER THICKNESS UNIFORMITY IN THERMAL NANOIMPRINT LITHOGRAPHY: EVALUATING STAMP CAVITY-HEIGHT AND 'DUMMY-FILL' SELECTION STRATEGIES

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We use chip-scale thermal nanoimprint simulations to show that the addition of non-functional 'dummy' features to a realistic integrated-circuit stamp design can substantially improve both residual layer thickness (RLT) uniformity and the completeness of stamp cavity filling at the end of a given nanoimprint process. We also show that although an arbitrarily small average RLT can be obtained if stamp cavities are tall enough *not* to fill with resist, unfilled cavities do not necessarily guarantee minimal RLT *variation* — the quantity that is key to controlling critical dimensions of structures that might subsequently be etched using the imprinted pattern as a mask.

To help elucidate nanoimprint pattern dependencies, we have used our previously described fast simulation technique, which we have validated experimentally [1, 2], to model imprinting by a silicon stamp whose features are arranged in long, parallel stripes of alternating protrusion density (Fig 1). The stamp's cavity height, h, is chosen so that complete cavity-filling occurs with an average RLT of one-third the mask regions' average thickness. For stripe widths, W, up to a few tens of micrometers, the time for cavities to fill completely with resist scales as W^2. For larger W, stamp deflections enable early cavity filling near the center of lower-density stripes, and filling time falls towards a value that depends on the density contrast, $\Delta\rho$, between stripes. Meanwhile, the amplitude of any spatial RLT variation decays exponentially with imprint time. With polymeric stamps, which are ~100 times less stiff than silicon, stamp deflections for a given pressure are larger and allow far faster cavity-filling, and RLT variation would likely dominate.

We also find (Fig 2) that a reasonable approximation to the cavity-filling time of a pattern may be provided by extracting, for a few values of W, the maximal density difference $\Delta\rho$ between any two abutting $W\times W$ regions of the pattern, and summing the times that our model of Fig 1 predicts for all chosen W and their corresponding extracted $\Delta\rho$. This approach is able to describe the filling times of randomly generated 'patchwork' patterns to within a factor of five across two orders of magnitude. Such an estimator of imprint time could be used to drive dummy-fill placement.

To investigate the relevance of dummy-fill placement and cavity-height selection in a real design, we have simulated the imprinting of the Metal-1 layout of an integrated circuit, including a large sea of custom-designed logic and a full pad-ring. Feature-area and -perimeter densities have been extracted from the chip's layout on a 3.75-μm grid. A characteristic feature diameter is inferred for each region of the grid from the extracted densities. Our simulation technique captures both feature size and density dependencies, and so can simulate the initial filling of cavities as well as subsequent homogenization of RLT as resist flows laterally over distances of many micrometers.

If cavities are shallow enough to fill with resist during imprinting, setting the pattern density of each region of the grid as close as possible to the chip-average substantially reduces the peak transient range of RLT (Fig 3, case A). Complete cavity filling is also achieved earlier than without the addition of 'dummy fill'. Meanwhile, if cavities are tall enough never to fill (cases B and C), RLT naturally approaches a much smaller average value. If, however, stamp-average pressure is maintained at the same 5 MPa level as in the cavity-filling case, the peak transient RLT range is much larger. Even reducing the pressure by a factor of 10 results in an RLT range that is less favorable than case A with dummy fill. We conclude that if the etch-selectivity of the resist allows for an appreciable average RLT, uniformity may be best served by filling cavities and employing dummy fill. **Word Count:** 618

References:

[1] H. Taylor and D. Boning, "Fast simulation of pattern dependencies in thermal nanoimprint lithography," presented at Nanoimprint and Nanoprint Technology Conf., San Jose, CA, USA: 2009.
[2] H. K. Taylor and D. S. Boning, "Toward Nanoimprint Lithography-Aware Layout Design Checking", *Proc. SPIE*, vol. 7641, 764129, 2010.

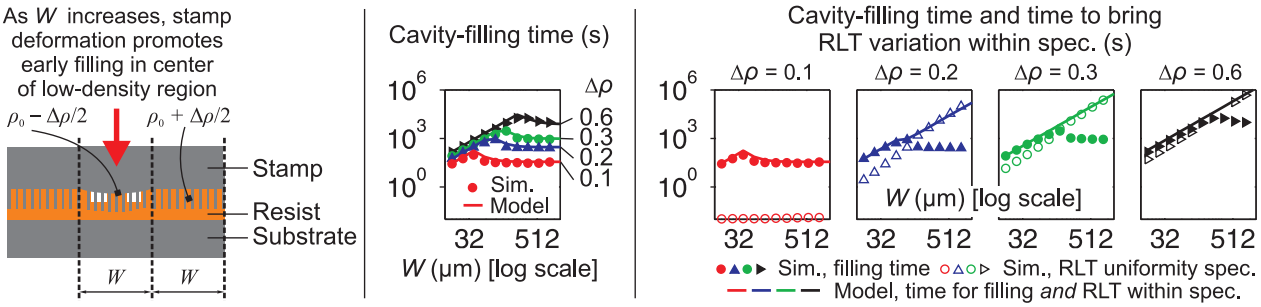

Fig. 1 Simulation and abstracted model of the imprinting of parallel stripes of alternating protrusion density. A silicon stamp, a resist viscosity of 10^4 Pa.s, and a stamp-average pressure of 5 MPa are assumed. Times for cavities to fill and for RLT to fall to within an 8.2 nm range are separately modeled. Other RLT uniformity specifications could be modeled. Feature sizes here are far smaller than W and do not affect simulated times.

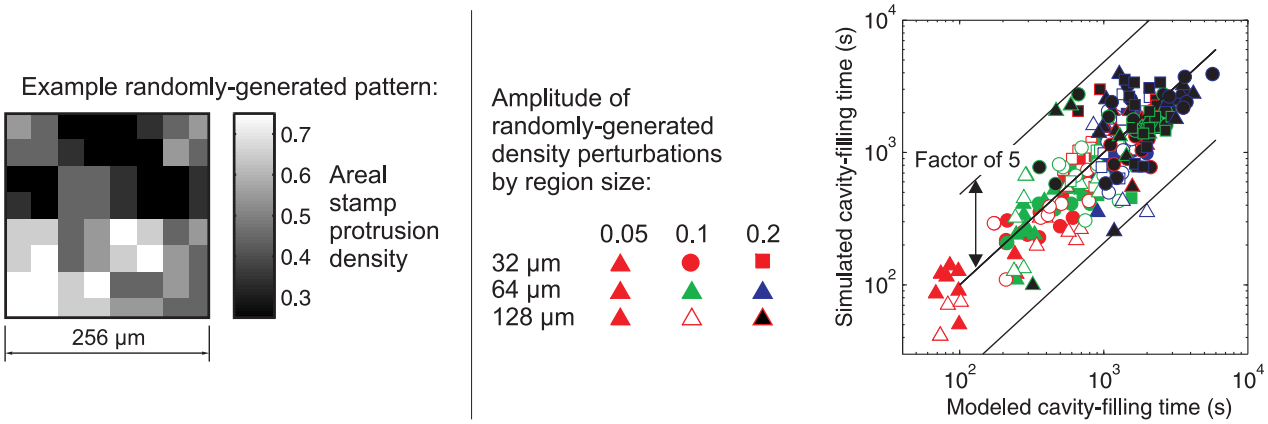

Fig. 2 Density patterns were randomly generated and cavity-filling times simulated. Maximal density gradients were extracted from each pattern at three length-scales: 32, 64 and 128 μm. The sum of the filling times predicted by the model of Fig 1 for the extracted densities at each of the three length-scales agrees with simulated filling time to within a factor of five, spanning two orders of magnitude.

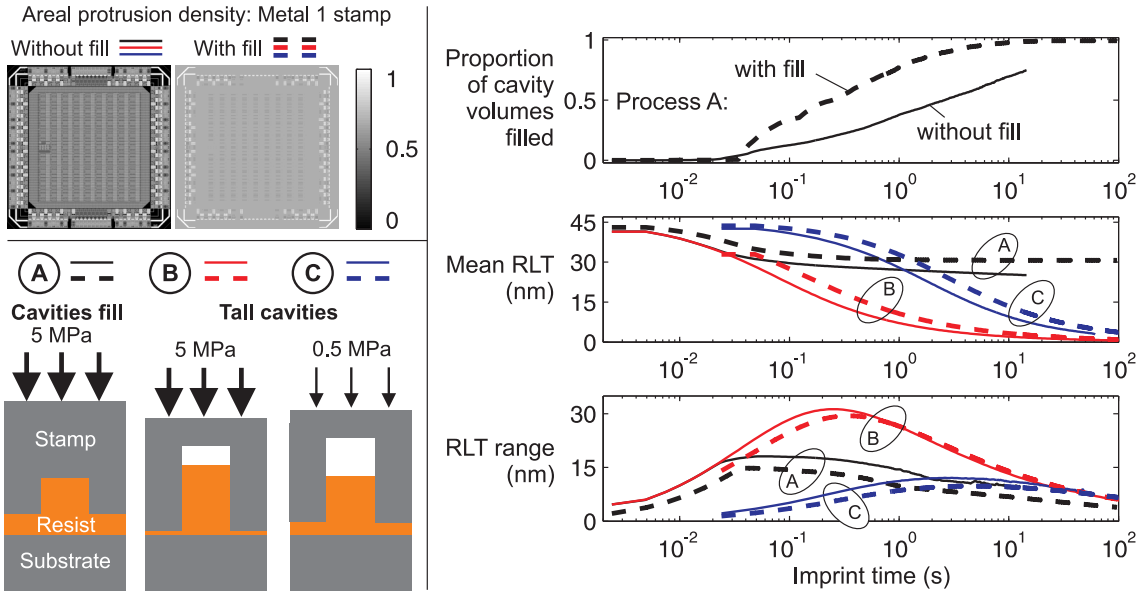

Fig. 3 Simulations of RLT evolution for the imprinting of a 940 μm-square Metal-1 pattern with a minimum feature size of 45 nm. Three cases are considered: (A) cavity relief 45 nm; stamp-average pressure, $p_0 = 5$ MPa; (B) cavities too tall to fill; $p_0 = 5$ MPa; (C) cavities as case B; $p_0 = 0.5$ MPa. For each case, results with and without density-homogenizing dummy fill are shown. The tightest eventual RLT range is obtained for case A with dummy fill. Stamp material: Si. Resist viscosity: 10^4 Pa.s. Initial resist thickness: 45 nm.